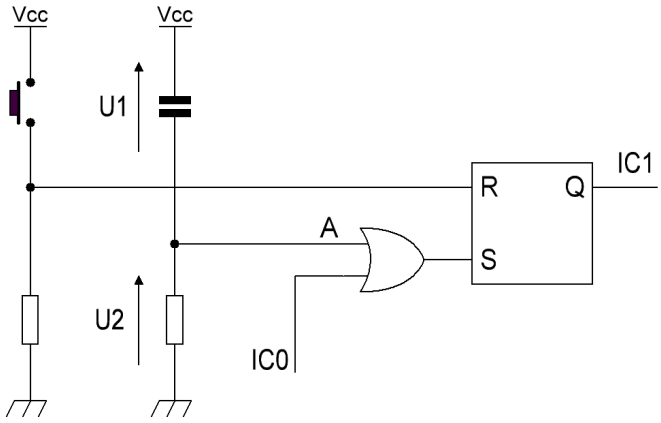
Tutorial 5
ROM Reading

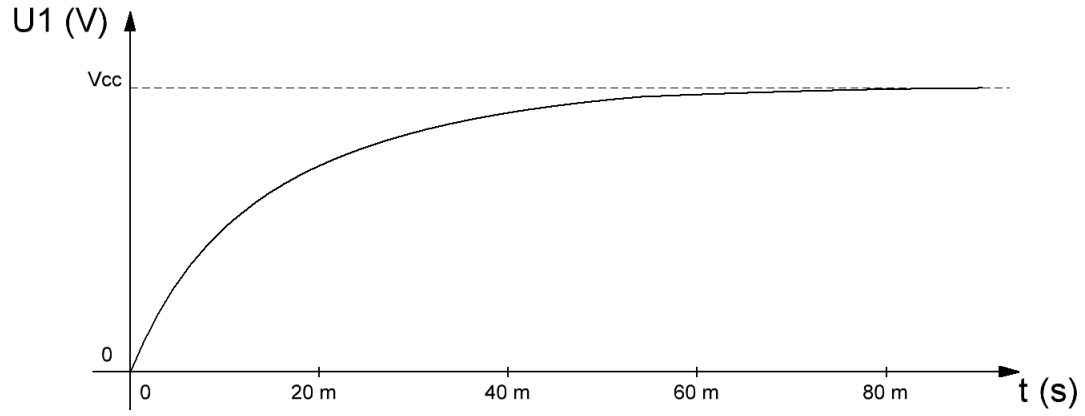
Part 1: Initialization and Control



Indications:

- The push-button is released when the power supply is switched on.
- Push-button released → R = 0.
- Push-button pressed → R = 1.
- The threshold voltage is Vcc / 2.
- The *A* logical state interpreted by the OR gate is 1 when *U2* is greater than the threshold voltage and 0 when *U2* is lower than the threshold voltage.

Timing diagram of the voltage across the capacitor:



1. Draw the voltage timing diagram of *U2* and the logic timing diagram of *A*.
2. Write down the value of *S* for the transient state (at the time of power-up) and the steady state (approximately 10 ms after power-up).
3. Assuming that the initial state of *IC0* is 0, what is the initial state of *IC1*?
4. Assuming that the circuit has reached the steady state, that $R = S = 0$ and that $IC1 = 1$, how can *IC1* be set to 0?
5. Assuming that the circuit has reached the steady state, that $R = S = 0$ and that $IC1 = 0$, how can *IC1* be set to 1?

Part 2: The Counters

The purpose of this part is to design two counters: an 11-bit binary counter and a 4-bit modulo-10 counter labeled **C1** and **C2** respectively. The **74HCT193** and **74HCT192** devices should be used to build these two counters (see datasheet). The outputs of **C1** and **C2** are labeled *Q10:0* and *Q'3:0* respectively. The clock signals of **C1** and **C2** are labeled *CK1* and *CK2* respectively.

6. How many **74HCT193** are necessary to build **C1**?
7. Find out the other ways of naming the inputs *C3*, *2+*, *1-* and *R*. Give the function of each input and output of the chip.
8. Draw a circuit diagram for **C1**, assuming that it continuously cycles through the natural binary sequence.
9. Using the circuit investigated in part 1, wire the **74HCT193** counters shown on the answer sheet in order to meet the following conditions:
   - The outputs of **C1** should be set to 0 when the power supply is switched on.
   - **C1** should start counting after a press of the push-button.
   - **C1** should stop counting once it has returned to zero.
10. Wire the **74HCT192** on the answer sheet so that **C2** counts only when **C1** counts. When **C2** does not count, its outputs should be 0. Apart from the modulo, the **74HCT193** and **74HCT192** counters are similar.

Part 3: Reading the ROM

After a press of the push-button, all the addresses of the ROM (**M2716**) should be read; that is to say all the data stored in the ROM should be placed successively on its data bus.

11. Using the **M2716** datasheet, wire each input of the ROM shown on the answer sheet.

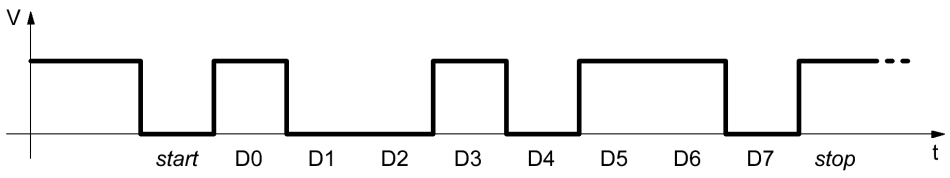
Part 4: Serial Transmission

The purpose of this part is to transfer the contents of the ROM through an RS-232 serial link.

Bitstream pattern:

- Start bit value: 0
- Number of data bits: 8
- Stop or idle bit value: 1
- Transmission rate: 9,600 baud

Bitstream example:
$D = 01101001_2$



The **MM74C150** multiplexer (see datasheet) should be used to perform the parallel-to-serial conversion.

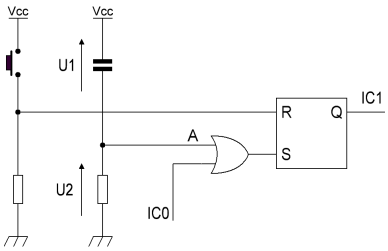
12. What should be placed on the output of the multiplexer?
13. How many input data lines of the multiplexer are required?
14. Assuming that $A = B = C = D = 0$ when no data is being transmitted, wire the input data lines of the multiplexer shown on the answer sheet in order to generate a proper bitstream.
15. The multiplexer should be controlled by the outputs of **C2**. Complete the wiring of the multiplexer.
16. What is the operating frequency of *CK2*?

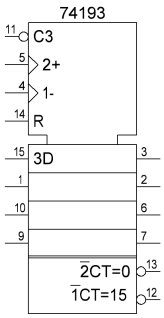
The byte being transmitted should remain on the ROM data bus until all of its bits are transmitted. Once the whole byte has been transmitted, the next byte can then be placed on the data bus.

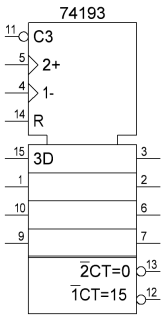
17. Which pin should *CK1* be connected to?
18. How long will the transmission of the whole memory last?

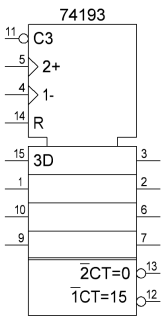
In order to reduce the number of silicon chips, all the gates and latches of this circuit will be replaced by NOR gates.

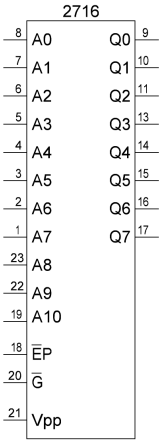
19. Draw the new circuit diagram.

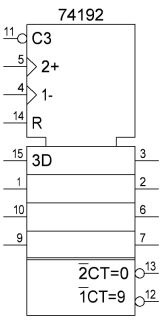

Vcc
Vcc
U1
U2
R
Q
S
A
IC1
IC0

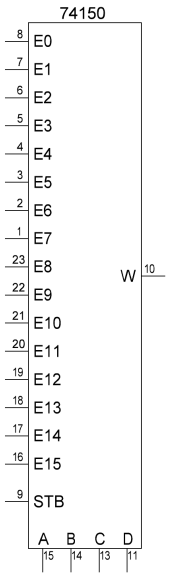

74193
C3
2+
1-
R
3D
2CT=0
1CT=15


74193
C3
2+
1-
R
3D
2CT=0
1CT=15


74193
C3
2+
1-
R
3D
2CT=0
1CT=15


2716
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
EP
G
Vpp
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7


74192
C3
2+
1-
R
3D
2CT=0
1CT=9


74150
E0
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
STB
A
B
C
D
W

Presettable synchronous 4-bit binary up/down counter

74HC/HCT193

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The “193” contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two’s or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.

$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input(1)
5	CP_U	count up clock input(1)
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

Note

1. LOW-to-HIGH, edge triggered

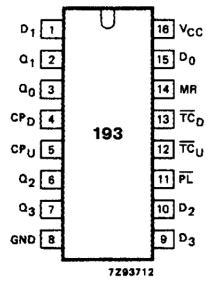


Fig.1 Pin configuration.

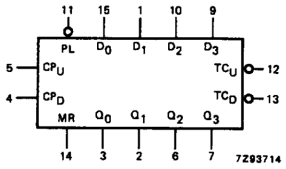


Fig.2 Logic symbol.

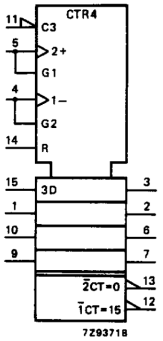


Fig.3 IEC logic symbol.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H H	X X	X X	L H	X X	X X	X X	X X	L L	L L	L L	L L	H H	L H
parallel load	L L L L	L L L L	X X L H	L H X X	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	H H L H	L H H H
count up	L	H	↑	H	X	X	X	X	count up				H[2]	H
count down	L	H	H	↑	X	X	X	X	count down				H	H[3]

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
2. $\overline{TC}_U$ = CP_U at terminal count up (HHHH)
3. $\overline{TC}_D$ = CP_D at terminal count down (LLLL)

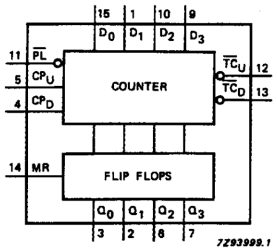


Fig.4 Functional diagram.

(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input (CP_D) must be HIGH, when counting down the count up clock input (CP_U) must be HIGH.

Sequence

Clear (reset outputs to zero);

load (preset) to binary thirteen;

count up to fourteen, fifteen, terminal count up, zero, one and two;

count down to one, zero, terminal count down, fifteen,

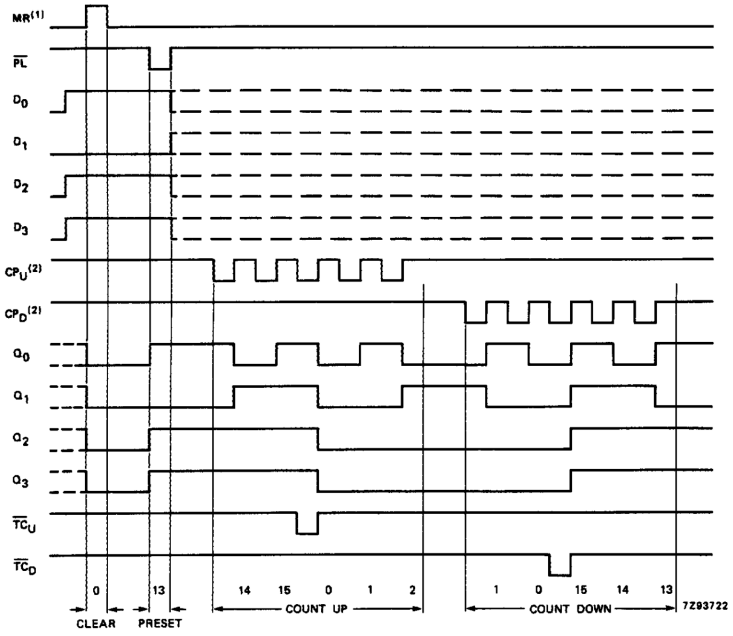


Fig.5 Typical clear, load and count sequence.

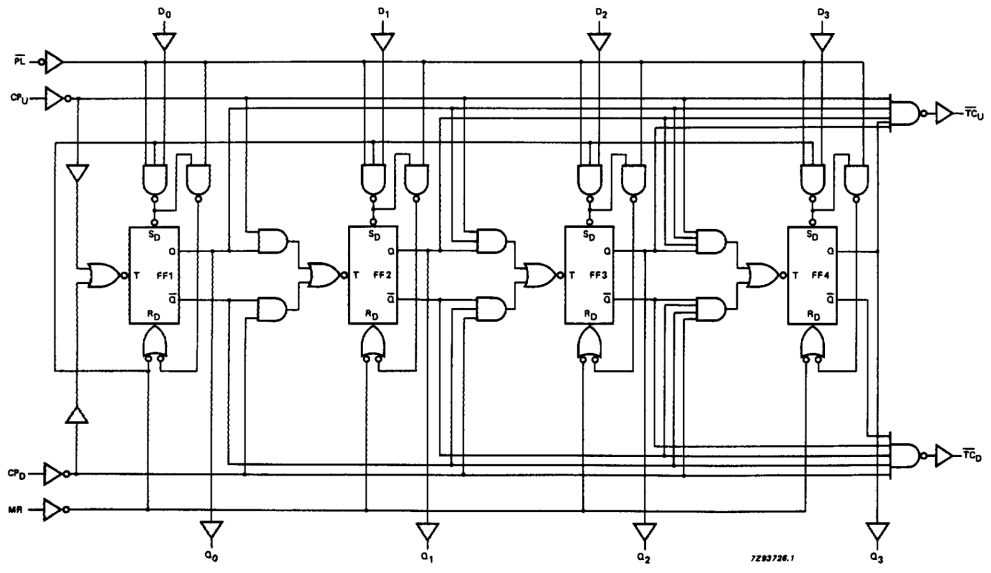


Fig.6 Logic diagram.

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised May 2002

MM74C150 • MM82C19
16-Line to 1-Line Multiplexer 3-STATE • 16-Line to 1-Line Multiplexer

General Description

The MM74C150 and MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM74C150 in the logical “1” state and the output of MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

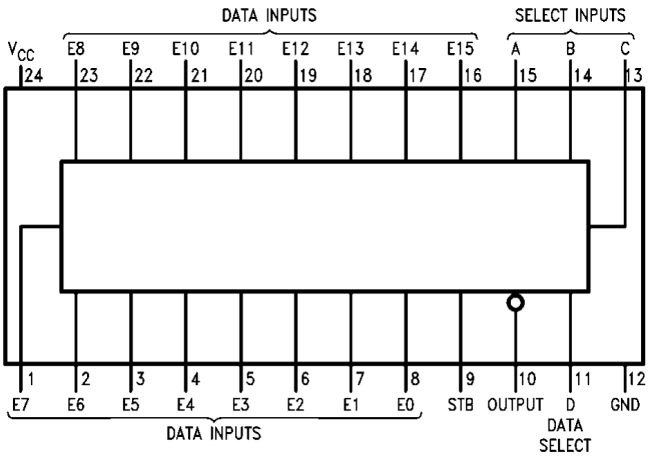
Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- TTL compatibility: Drive 1 TTL Load

Ordering Code:

Order Number	Package Number	Package Description
MM74C150N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
MM82C19N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Connection Diagram



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Truth Table

MM74C150

Inputs																				Output
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 (Note 1)
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

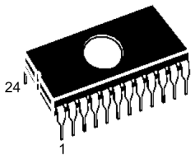
Note 1: For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

SGS-THOMSON MICROELECTRONICS

M2716

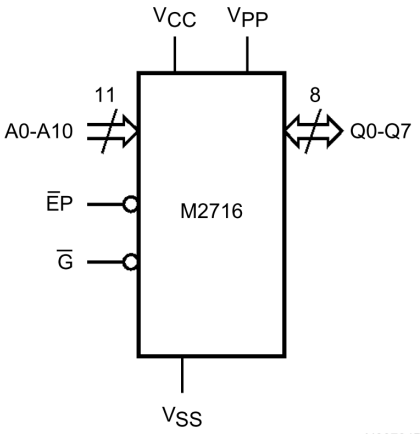
NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525mW Max ACTIVE POWER, 132mW Max STANDBY POWER
- ACCESS TIME:
  - M2716-1 is 350ns
  - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS and OUTPUTS TTL COMPATIBLE DURING BOTH READ and PROGRAM MODES
- THREE-STATE OUTPUT with TIED-OR-CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V



FDIP24W (F)

Figure 1. Logic Diagram



DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

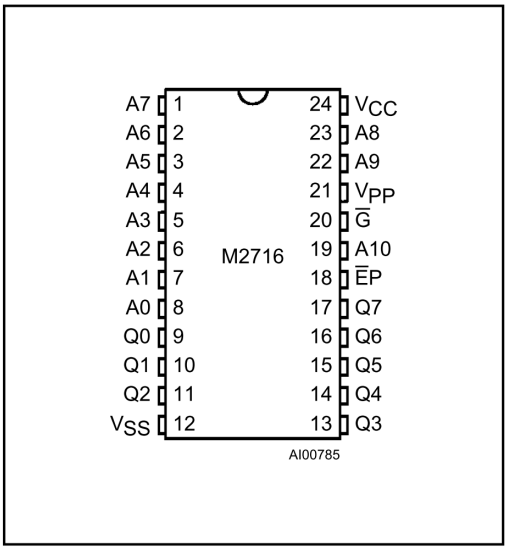
A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}P$	Chip Enable / Program
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{CC}	Supply Voltage		–0.3 to 6	V
V_{IO}	Input or Output Voltages		–0.3 to 6	V
V_{PP}	Program Supply		–0.3 to 26.5	V
P_D	Power Dissipation		1.5	W

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\overline{G}$ = V_{IL}, $\overline{EP}$ = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV}, t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\overline{G}$ = V_{IH}. This mode is independent of $\overline{EP}$ and the condition of the addresses. The outputs are Hi-Z when $\overline{G}$ = V_{IH}. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\overline{EP}$ = V_{IH}. This is independent of $\overline{G}$ and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{EP}$ pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with V_{PP} = 25V, V_{CC} = 5V, $\overline{G}$ = V_{IH} and $\overline{EP}$ = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{G}$ = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

Mode	$\overline{EP}$	$\overline{G}$	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.